

Calibration of Inductance Calculations to Measurement Data for Superconductive Integrated Circuit Processes

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Abstract—It is easy to adjust the parameters for field-solver inductance extraction models to fit a single measurement. However, more effort is required to calibrate a model for a representative collection of line widths, layers and fabrication runs. Numerically calculated inductance is also a strong function of segment size. A segment size is selected to optimize extraction accuracy versus speed for large RSFQ logic cells. InductEx is then calibrated for this segment size. Measured data from 54 test structures of different widths and layers, repeated on many chips over 22 wafers of Hypres’s 4.5 kA/cm² mask aligner process and 48 test structures from 5 wafers for the wafer stepper process were used to find the Hypres process averages. Artificial changes to InductEx layer parameters such as mask-wafer bias and penetration depth are used to first reduce skew between results for different widths, and then differences between layers. This results in a set of calibrated process parameters for inductance calculations with InductEx for both the mask aligner and wafer stepper processes from Hypres. Calibrated inductance calculation results agree with the average measurements with a root mean square error (RMSE) smaller than 2.3 % over the full range of line widths from 0.8 μm to 20 μm, showing InductEx as a useful tool for narrow-line inductance calculations.

Index Terms—Calibration, InductEx, layout extraction, numerical inductance calculation, segment size.

I. INTRODUCTION

THE importance of inductance calculation for the layout of superconductive electronic (SCE) circuits has been discussed many times [1]-[4].

Manufacturing processes (especially for low temperature superconductors) are characterized thoroughly, and reliable sheet inductance values (inductance per square) are sometimes published, such as that for the Hypres 4.5 kA/cm² niobium process [5]. Such sheet inductance values are useful for the quick design of straight-line inductance sections, but for complex circuit structures [6]-[8], mixed-signal and large-scale circuits [9]-[11] a numerical inductance calculation tool is required.

Numerical inductance calculation tools (many of which

exist for superconductive integrated circuit structures [12]-[16] are never completely accurate, but approach analytical results for arbitrary small segment size. (Modeling technique also plays an important role in accuracy [13]). However, small segment size, especially in 3D solvers, is very expensive in terms of calculation time and system memory. From an engineering perspective, numerical calculation parameters should thus be chosen to balance calculation time and accuracy over the entire range of feature sizes in a typical layout extraction problem.

In this paper, we show that calculations with FastHenry [17], [18] (used as a field solver by InductEx [13], [19], which creates segmented models from GDSII or similar layout files) can be calibrated to use a single, coarse segmentation size and still yield results within a defined error over an entire line width range. We use the 4.5 kA/cm² niobium process of Hypres [20], and calibrate for two manufacturing techniques: a mask aligner and a wafer stepper.

II. MODEL AND PROCESS PARAMETERS

In numerical models, every parameter influences

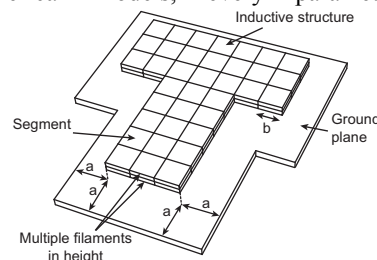


Fig. 1. Model parameters for an inductive structure over a ground plane in InductEx. The ground plane is automatically clipped to the overhang parameter a , while structures are divided into segments with side length b and each segment into a number of height filaments. For clarity, ground plane segmentation and x - y segment interleaving [22] are not shown.

TABLE I
HYPRES LAYER DEFINITIONS AND NOMINAL PROCESS PARAMETERS [20]

Description	Name	Thickness (nm)	λ (nm)	Bias (μm)
Ground	M0	100	90	0.2
Isolation	I0	150	-	0.2
First wiring layer	M1	135	90	0
Isolation	I1B	200	-	-0.1
Second wiring layer	M2	300	90	-0.2
Isolation	I2	500	-	0.2
Third wiring layer / skyplane	M3	600	90	-0.4

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calculation results – not just the physical parameters of the process (the process parameters, Table 1), but also tool-specific parameters that control modeling (the modeling parameters, Fig. 1). Parameters should thus be used consistently to prevent deviations in results between different calculations. The important tool-specific parameters for InductEx are segmentation size, ground plane overhang and layer filamentation (see Fig. 1). These parameters largely determine calculation speed.

The nominal parameters for the Hypres 4.5 kA/cm² process [20] are shown in Table 1 (for the mask aligner), and are used as default in the layer definition file that describes the process to InductEx [21]. These parameters are line and isolation thickness, London penetration depth (λ) and the mask-to-wafer bias (offset), which together primarily determine calculation accuracy.

III. CALIBRATION

A. Objective

The objective of a calibration sequence for InductEx is to determine a set of artificial process parameters for any given set of modeling parameters that would yield the smallest error between calculated and measured results over the full range of

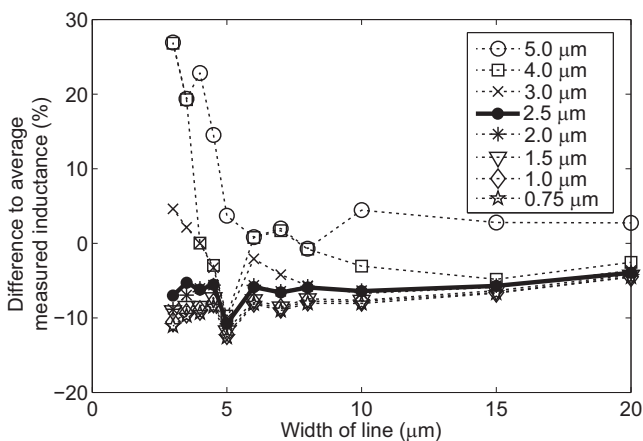


Fig. 2. Difference between InductEx calculations and average measurements from 22 wafers of per-length inductance in the Hypres 4.5 kA/cm² process (using a mask aligner) for various segment sizes. Lines are in M1. Nominal process parameters are used.

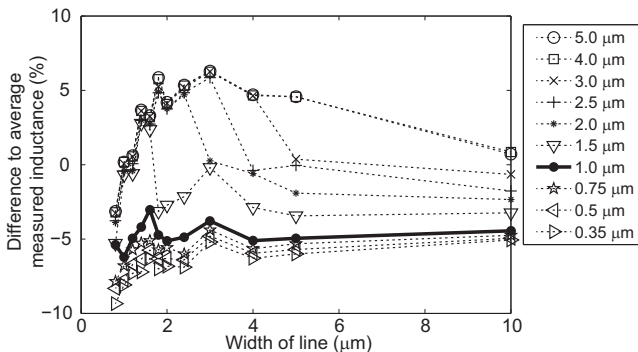


Fig. 3. Difference between InductEx calculations and average measurements from 5 wafers of per-length inductance in the Hypres 4.5 kA/cm² process (using a wafer stepper) for various segment sizes. Lines are in M1. Nominal process parameters are used.

line widths used for layout in a process. Such calibration requires a thorough set of measured data over many wafers, which is available for Hypres [5] over a range of line widths from 3 μm to 20 μm for the mask aligner process and 0.8 μm to 10 μm for the wafer stepper process.

It is very important to note that the calibrated process parameters are completely artificial, and by no means reflect on the actual manufacturing process, but rather on the numerical model. Several sets of very different parameter values will yield good calculation results over the range of geometries studied.

B. Fixing the model parameters

The first step in the calibration sequence is to determine model parameters that yield the fastest solution time and acceptable consistency. As an example, consider segmentation size (for a detailed description of segmentation, see [22]). The difference between InductEx calculations (using nominal process parameters) and average measurements from 22 wafers of per-length inductance in the mask aligner process (with lines in M1) for various segment sizes is shown in Fig. 2. Inductance measurements are obtained from automated SQUID modulation tests [23], with each inductive structure forming the loop inductor of a SQUID. It is evident that the choice of segment size determines whether calculation results are higher or lower than measurements. Once segmentation size is fixed, it is this difference that must be nullified through process parameter adjustments. For segment size 3 μm and above, the calculation error increases sharply at lower line widths (this is mostly due to the coarse modeling of current distribution in the ground plane beneath lines). The largest segment size with a flat error curve is 2.5 μm (thick black line in Fig. 2), and this is fixed as the model parameter for the mask aligner process. We obtain the same results for lines in other layers. The ground plane overhang (2.5 μm) and filamentation number for each layer are similarly chosen.

Fig. 3 shows the InductEx calculation error to average measurements from 5 wafers manufactured with the wafer stepper process, where line width goes down to 0.8 μm . The largest segmentation size with a flat error curve is 1 μm (once again indicated as a thick black line in Fig. 3).

C. Process parameter adjustment sequence

The difference between InductEx calculations and measurements of per-length inductance for the mask aligner

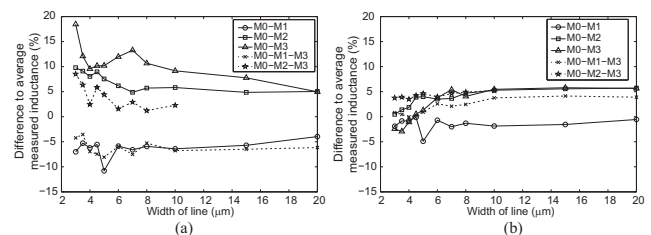


Fig. 4. Difference between per-length inductance for the Hypres 4.5 kA/cm² process using mask aligner (a) calculated with InductEx and nominal process parameters and (b) derived from average sheet inductance [5] to the average measurements from 22 wafers.

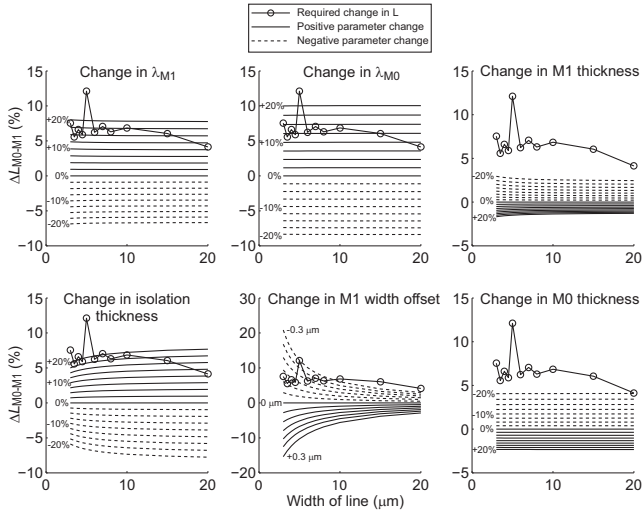


Fig. 5. Effect of parameter variations on M1 line inductance in the mask aligner process, with required shift in inductance to match measurements.

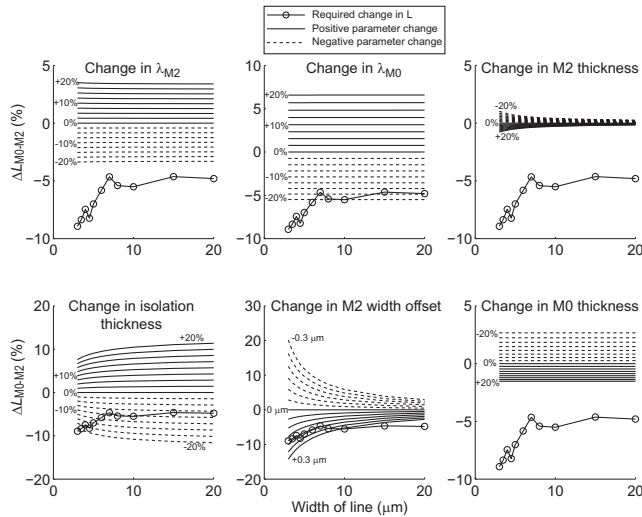


Fig. 6. Effect of parameter variations on M2 line inductance in the mask aligner process, with required shift in inductance to match measurements.

process, with a segmentation size of $2.5 \mu\text{m}$ and nominal process parameters (Table 1), is plotted in Fig. 4(a), and the equivalent difference between sheet inductance values [5] and measurements is shown in Fig. 4(b). The nominal (uncalibrated) root mean square error (RMSE) is 7.6 %, and the calibration goal is to make the InductEx error at least as small as the sheet inductance error. Inductance structures are in M1, M2 and M3 above ground (M0), as well as in M1 sandwiched between M0 and M3, and M2 sandwiched between M0 and M3 [5].

In order to choose process parameters to vary (and determine the magnitude of such variations), the required calibration shift in calculated inductance for each layer is plotted (layer M1 in Fig. 5, layer M2 in Fig. 6 and layer M3 in Fig. 7) together with the change in inductance calculated with Chang’s analytical equation [24] when 6 process parameters are varied. We use Matlab scripts to automatically generate these plots, and Chang’s equation allows us to quickly sweep through all parameter values.

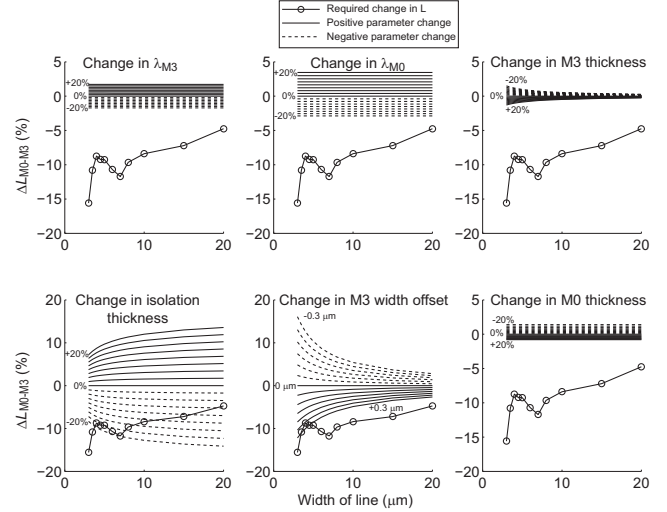


Fig. 7. Effect of parameter variations on M3 line inductance in the mask aligner process, with required shift in inductance to match measurements.

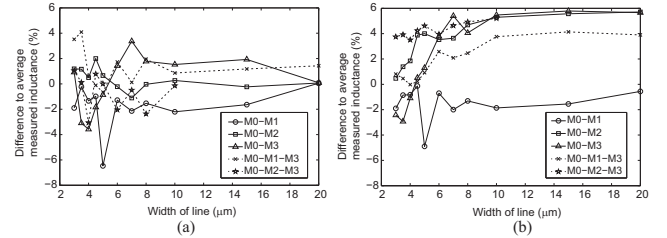


Fig. 8. Difference between per-length inductance for the Hypres 4.5 kA/cm^2 process using mask aligner (a) calculated with InductEx calibrated for $2.5 \mu\text{m}$ segment size and (b) derived from average sheet inductance [5] to the average measurements from 22 wafers.

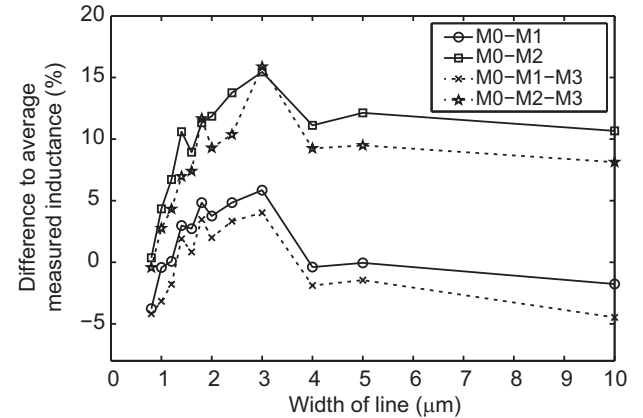


Fig. 9. Difference between per-length inductance for the Hypres 4.5 kA/cm^2 process using a wafer stepper calculated with InductEx for nominal process parameters and average measurements from 5 wafers. RMSE is 6.94 %

From Fig. 5, we now adjust width bias (mask-to-wafer) to the first negative line ($-0.05 \mu\text{m}$) to adjust curve skew, and λ_{M1} to the 6th positive line (103.5 nm) to minimize the error. Changes in line and ground plane thickness are not considered, because the effect is much smaller than that of width bias and λ_{M1} . Changing the value of λ_{M0} is also not considered yet, as it will affect the inductance of lines in M2 and M3 (we sometimes adjust it later to reduce the error for the sandwiched conductors).

Similarly (from Fig. 6), the width bias for M2 is increased

TABLE II

INDUCTEX PROCESS PARAMETERS FOR HYPRES MASK ALIGNER AND WAFER STEPPER PROCESSES [20], LISTED AS NOMINAL (NOM) AND CALIBRATED (CAL).

Description	Mask aligner		Wafer stepper		
	Nom	Cal 2.5 μm	Nom	Cal 2.5 μm	Cal 1 μm
λ_{M0} (nm)	90	78	90	75	90
λ_{M1} (nm)	90	112	90	97	99
λ_{M2} (nm)	90	97.5	90	70	60
λ_{M3} (nm)	90	110	90	95	90
BiasM1 (μm)	0	0.015	0	0	0
BiasM2 (μm)	-0.2	-0.1	-0.1	-0.15	-0.15
BiasM3 (μm)	-0.4	-0.05	-0.3	-0.3	-0.3
Thickness I0 (nm)	150	150	150	150	200
Thickness I1 (nm)	200	190	200	150	140
Thickness I2 (nm)	500	495	500	490	500

by 0.1 μm and λ_{M2} reduced by 12.5 %, while the width bias of M3 is increased by 0.25 μm and the isolation thickness (I2) decreased by 5 % (from Fig. 7). The RMSE between InductEx and measurements over all structures is now reduced to 3.06 %. The cycle is repeated a few times (we create updated parameter variation plots to identify new variation options) to yield an optimized process parameter set as shown in Table 2. The final RMSE is 1.87 %. The error for different layers as a function of line width is shown in Fig. 8(a), and it is smaller than the error between the published average sheet inductance values for the process [5] and measurements (which is repeated in Fig. 8(b) for comparison).

Although not shown here, we also consider the error in the sandwiched inductance structures (M0-M1-M3 and M0-M2-M3) during the final adjustment cycle.

A similar calibration sequence is performed for the wafer stepper process. The uncalibrated error between InductEx and average measurements is shown in Fig. 9 (with an RMSE of 6.94 %), while the calibrated error is shown in Fig. 10 (with an RMSE of 2.25 %).

IV. RESULTS

Calibration of the process parameters reduces the RMSE between InductEx calculations and average measured results for the Hypres 4.5 kA/cm² process to 1.87 % for the mask aligner and 2.25 % for the wafer stepper. These parameters are shown in Table 2, together with nominal process parameters.

Table 2 also shows a calibration result for the mask aligner when a segment size of 2.5 μm is used. Although this segment size gives solutions that are on average 7 times faster than with 1 μm segment size, the RMSE is increased to 3.25 %.

The calibration parameters for a range of segmentation sizes can (and should) be updated after every wafer run, and currently we provide the latest version (with updates) on the InductEx homepage [19].

V. CONCLUSION

We show that InductEx is a useful tool for the calculation of superconductive integrated circuit inductance even at small line widths as employed in a wafer stepper process from

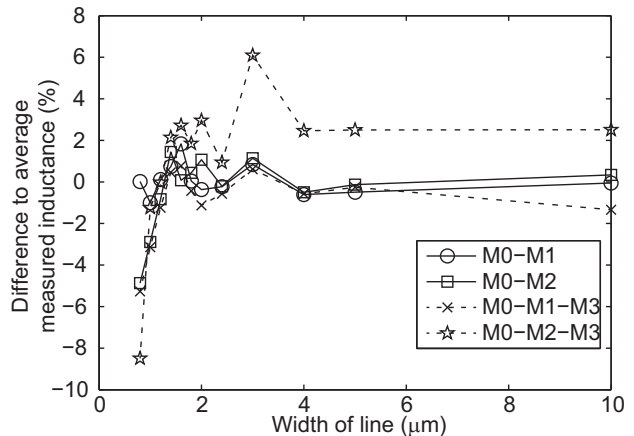


Fig. 10. Difference between per-length inductance for the Hypres 4.5 kA/cm² process using a wafer stepper calculated with InductEx for calibrated process parameters (with 1 μm segment size) and average measurements from 5 wafers. RMSE is 2.25 %.

Hypres. With calibration, the RMSE of InductEx to average measured values over many wafers can be made small – lower than 2.3 % for the Hypres processes.

If smaller calculation inaccuracies are required, the calibration process can be repeated for smaller segment sizes, at the cost of increased computation time.

It should be noted that many process parameter sets can be found to produce similarly low errors between calculations and measurements, but by selectively tuning parameters over limited ranges, we aim to find a set for which the differences between calibrated and nominal process parameters are as small as possible.

We also aim to gather equally comprehensive data for other fabrication processes and then develop a generic automated parameter calibration and error minimization algorithm.

Although the calibration structures discussed here are all straight microstrip lines, recent experiments (using a much smaller calibration set of straight microstrip lines for the RSFQ niobium process from IPHT Jena [25]) showed that such calibration results in very good agreement between calculations and measurements for other straight-line structures [13], more complex layouts (meanders and ground plane holes) [26] and very complex layouts (split ground planes and hole-assisted coupling of inductors with multiple bends) [6].

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