SFQ Circuits with Ground Plane Hole-Assisted Inductive Coupling Designed with InductEx

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Abstract—The design of single flux-quantum (SFQ) circuits requires well-defined inductances. In many cases these are created by irregular geometries and a computer aided design tool is necessary for inductance calculations. This becomes a challenging task in cases where no ground plane is used and thus three-dimensional calculations are required. For this purpose, InductEx was developed and verified successfully for simple structures. In this work we take the next step and demonstrate the applicability of InductEx to the design of Rapid Single Flux-Quantum (RSFQ) cells. We use InductEx for inductance modeling as an integral part of the design cycle for an RSFQ cell with flux quantum transfer via mutual inductance and for a DC-reprogrammable logic circuit with similar inductive coupling. The relation between coupling factor and self-inductance is optimized in the circuit layout. All coupling structures are duplicated in SQUID modulation test circuits to measure and verify calculation accuracy. We find excellent agreement between the calculated and measured inductance values. Furthermore, the operational area of the basic cell is determined and compared with similar investigations reported earlier. Based on this comparison we conclude that InductEx is a valuable inductance design tool, and that mutual coupling in structures using ground plane holes and RSFQ-compatible self-inductances can be modeled and designed reliably.

Index Terms—Current recycling, dc-reprogrammable logic, ground plane holes, inductance calculations, InductEx, inductive coupling, layout extraction, low-power RSFQ, LR-biasing, serial biasing.

I. INTRODUCTION

RAPID Single Flux Quantum (RSFQ) circuits (and SFQ circuits in general) are composed of three elemental building blocks: resistors, Josephson junctions and inductances [1]. For physical layout, the resistors and junctions are implemented as regular simple structures, resulting in linear or quadratic relations respectively between their dimensions and realized values.

The inductances are in many cases defined by microstrip line configurations and perform two tasks in an RSFQ circuit: they realize electrical connections and galvanic coupling between circuit parts and define the functionality of circuit sections (storing or propagating flux quanta). Due to long or sometimes very short distances between circuit nodes, inductances in many cases have no regular layout geometries and need to be designed carefully to implement the desired storing behavior of a loop. Therefore inductance calculation is important for the design of RSFQ circuits.

Calculation accuracy, calculation time and the integration of a tool into the design flow are important aspects for efficient circuit design. For two-dimensional (2D) inductance extraction, Lmeter [2] is fast and sufficiently accurate, and is mostly used. However, in cases where three-dimensional (3D) inductance extraction is required, an adequate tool (especially in terms of design flow integration) was not available. To address this, InductEx [3] was developed to provide a user-friendly interface to FastHenry [4] (itself modified to handle multi-terminal superconductive structures [5]). Firstly we analyzed the accuracy of InductEx for extraction of 2D circuit inductances [3]. Next the applicability of InductEx to simple 3D problems was analyzed through the investigation of lines crossing ground plane holes [6], and its accuracy was again confirmed.

In this work we take the next step and demonstrate the applicability of InductEx to the design of RSFQ basic cells with advanced 3D inductance layouts. When RSFQ circuits contain magnetically coupled components (through mutual inductance), a ground plane is necessary to realize low self inductances. However, a ground plane severely limits the coupling factor. If a high coupling factor ($k > 0.5$) is required, strategically placed ground plane holes can be used to improve mutual inductance, and inductance extraction then requires a 3D tool. Here we demonstrate through two examples – an inductive pulse transfer (TX) cell and a DC-resettable latch (DCRL) – that InductEx has the required abilities to design such circuits successfully. We used LASI [7] and LayoutEditor [8] (with macro support for InductEx) for circuit layouts discussed here. Layouts are sent to InductEx in GDSII format. Detail on InductEx modeling procedures and integration with CAD tools is available in the user’s manual [9].

II. INDUCTIVE COUPLING IN RSFQ CELLS

Power dissipation in single-flux-quantum (SFQ) circuits is an important design issue for large systems, hence the
An inductively coupled transmission cell (TX cell) was designed according to that presented by Johnson et al. [17] to inject an incoming single flux quantum (SFQ) pulse into a resistively terminated transformer. The circuit schematic diagram is shown in Fig. 1, with $L_4$ as the primary inductance of the transformer and $L_5$ the secondary inductance. As with other published transmission cells [18], [19], [22], the receiver side of the TX cell is triggered asynchronously by the driver side, and is therefore not clocked.

### B. DCRL

The DC-Resettable Latch is a key component of a proposed superconductive programmable gate array [24], and was presented (with simulated response) earlier [28]. The DCRL was redesigned and optimized for the niobium RSFQ process of IPHT, and the schematic circuit diagram is shown in Fig. 2. The dc reset current is 790 $\mu$A, and simulated bias margins at 10 GHz are listed in Table 1. Coupling between the dc reset line and the storage inductor $L_{2b}$ was strengthened through the use of a ground plane hole, as described below.

### III. CIRCUIT DESIGN

#### A. TX cell

Careful design of the coupling between inductors $L_4$ and $L_5$ is necessary to keep self-inductance low for both inductors, while maximizing the mutual inductance. Johnson et al. [17] used a ground plane tongue, extending over a ground plane moat that isolates the driver and receiver sections, to minimize self-inductance. Mutual inductance was improved with a ground plane hole underneath the transformer. A detailed analysis of different techniques by Igarashi et al. [22] confirmed that the former is by far the most effective.

Due to differences between manufacturing processes, the layout described above is not exactly reproducible in the RSFQ niobium process of IPHT. We designed a layout that preserves low inductance for both $L_4$ and $L_5$, while allowing coupling to $L_{2b}$ of the DCRL should be as strong as possible.

Finally, to verify the accuracy of the calculated inductance and coupling in these layouts, we manufactured SQUID test structures with which to measure the inductance of similar coupling structures (through SQUID modulation [27]) for comparison to calculations.

### IV. INDUCTANCE DESIGN AND LAYOUT

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strong coupling over a ground plane hole. The layout is shown schematically in Fig. 3(a), with a cross-section detailing the use of a ground plane tongue in the second wiring layer (M2) shown in Fig. 3(b). The ground plane tongue (that brings the driver side ground plane over to the receiver section) is not continuously seamed on the driver side the way that Igarashi et al. do it, but only connected through two vias as shown in Fig. 3(a) to conserve layout space. A microphotograph of the manufactured circuit is shown in Fig. 4.

B. DCRL

Due to differences between the RSFQ niobium processes of IPHT and Hypres, the DCRL layout in [28] cannot be exactly duplicated in the IPHT process. We used a small ground plane hole (see the microphotograph of the manufactured circuit in Fig. 5) to strengthen coupling while keeping the inductance of $L_{2b}$ low. With InductEx [3], the mutual inductance is calculated as 4.5 pH (an improvement over the 3.9 pH in the older layout [28]).

V. RESULTS

A. Inductance tests

The segmented InductEx calculation model for the full TX cell is shown in Fig. 6. For a detailed explanation of InductEx’s segmentation algorithm, see [3], [29]. We used a maximum segment size of 2.5 μm for all calculation models. SQUID test structures were also manufactured to verify the inductance modeling and calculation method. However, the SQUIDs have bias lines, which in the case of the TX cell transformer intrudes over the ground plane hole, and in the case of the small hole of the DCRL’s transformer required us to use two equal ground plane holes on both sides of the bias line for symmetry. The SQUID results therefore do not directly reflect the inductances in the TX cell and DCRL, but are only used to verify the calculation method (InductEx
The results agree with those in Table 2, with the TX cell SQUID measuring the equivalent inductance \( L_1 \) (calculated through measurements and calculations on a set of process parameters used for InductEx calculations were also constructed for the SQUID test structures). Microphotographs of the SQUID test structures are shown in Fig. 7.

In order to compensate for fabrication tolerances, the process parameters used for InductEx calculations were calibrated through measurements and calculations on a set of test structures included on the wafer, as discussed earlier [3].

The SQUID calculation and measurement results are shown in Table 2, with the TX cell SQUID measuring the equivalent inductance \( L_1 \), and the DCRL SQUID measuring an equivalent of \( L_2 \) with two ground plane holes for symmetry. The results agree very well, and we obtain a very good ratio of mutual inductance over self-inductance.

To demonstrate conclusively that the layout with a ground plane tongue and ground plane hole that does not touch the isolation moat is a good solution, we modeled layouts without the ground plane tongue and with holes of varying sizes that touch the isolation moat, as shown in Fig. 8, and analyzed these with InductEx. (These structures were not manufactured). Similar to [22], we found these layouts to be suboptimal when compared to the layout in Fig. 3, as is evident from the results in Table 3.

### B. Circuit tests

Only the TX cell has been tested to date. An oscilloscope screenshot showing successful pulse transmission is shown in Fig. 9, and the measured bias current margins are listed in Table 4. The measured bias margins compare very well with the simulated margins, which is significant because the simulated critical margin \( I_{b2} \) is very narrow (and corresponds exactly to the critical margin reported by Kang et al. [18]). This demonstrates conclusively that the inductance design and verification process is reliable.

### VI. Conclusion

We show through measurements of manufactured circuits that inductive pulse transfer circuits with hole-assisted coupling can be modeled and designed reliably with the use of InductEx (inductance, coupling factor and bias current margins of measured circuits correspond very well to the design). However, the pulse transfer circuits still have very narrow margins, so that we will investigate the addition of a double-flux-quantum (DFQ) driver [31] (as implemented by Johnson et al. [17]) to widen the bias margins.

We also show that the TX cell coupling layout identified by Igarashi et al. as optimal [22] (and reported earlier by Johnson et al. [17]) is indeed so, and that it is possible to reproduce the coupling in the RSFQ niobium process of IPHT. However, using InductEx, we obtain a better agreement between calculated and measured inductance values (1% to 5%, as shown in Table 2) as well as a significantly higher ratio of mutual to self-inductance of the receiver section (0.71 to 0.75, compared to 0.63).

### REFERENCES


