Full-gate verification of superconducting integrated circuit layouts with InductEx

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Abstract—At present, superconducting integrated circuit layouts are verified through a variety of techniques. A layout-versus-schematic method implemented in Cadence allows extraction of circuit schematics with certain geometry-dependent parameters. Lmeter calculates inductance in a layout network, and with proper setup may also calculate resistance separately. Recently, InductEx was introduced to calculate multi-terminal network inductance in a superconductor structure with support for more complicated three-dimensional geometries. Here we present an improvement to InductEx that allows resistance, inductance and Josephson junction critical current extraction of a full superconducting digital logic gate or cell in a single execution, and in reasonable time. We show how InductEx was designed to operate on tape-out ready layouts, and through example how it is used for full-gate layout verification of contemporary logic cells.

Index Terms—Inductance extraction, InductEx, layout verification, three-dimensional modeling.

I. INTRODUCTION

Superconductive integrated circuit (IC) layouts, whether for Single Flux Quantum (SFQ) logic families such as RSFQ [1] and its energy efficient variations such as ERSFQ [2] and eSFQ [3], or other families such as AQFP [4, 5], are at present mostly verified only in part by computer. Cells laid out with software such as LASI [6], that does not link a circuit schematic to the layout, can have inductance verified with Lmeter [7] or InductEx [8] if a simplified circuit netlist is supplied to the calculator. However, manual verification of Josephson junction area and resistor layouts is still required. A more robust layout-versus-schematic method implemented in Cadence Virtuoso [9] allows verification of layouts against circuit schematics through geometry-dependent parameters and an interface to Lmeter, but the limitations of Lmeter and the cost of Cadence Virtuoso limit application.

Here we show how InductEx with resistivity support allows full-gate verification of parameter values in tape-out ready layouts without the need for back-annotated circuit schematics. We show that this allows even LASI layouts to be verified, and requires no complexity reduction that could impact on fabrication.

II. OVERVIEW OF INDUCTEX PROCESS FLOW

A quick overview of the InductEx process flow is required to explain some aspects of full-gate verification.

InductEx reads a circuit layout from industry-standard GDS (see [10] for a discussion on file structure) or CIF [11, 12] files, or from Lmeter or InductEx-specific DXC or IXI files [13]. These files only contain layout objects (such as polygons, rectangles and text labels) assigned to different layers. Some of these layout objects do not influence fabrication, but identify ports from which excitation voltages are to be applied for impedance calculation. InductEx assigns a positive and negative terminal to each port, as identified by labels.

A second input file is needed to provide fabrication-specific translation of the layout file to a three-dimensional (3D) calculation model. This layer definition file (or LDF file) lists layer numbers (for GDS) or layer names, as well as the order of fabrication. The 3D calculation model is constructed in the order of layer fabrication, and objects on conductive layers are populated with horizontal segments while objects on isolation layers establish via positions and allow inter-layer connectivity with vertical segments.

The circuit netlist, in a simplified Spice or JSIM [14] format, is read from a third input file. It consists of a list of inductive elements with design values and node numbers to establish connectivity, coupling elements that link inductors, and port elements of which the polarity of each terminal must agree with that specified in the layout file.

InductEx then translates the 3D model to the correct format for the numerical solver, executes the solver to calculate port currents, and solves element values in every branch in the circuit as discussed in Section 3C.

The output is a list of extracted parameter values that are compared with design values from the circuit netlist for inspection by the designer.

III. REQUIREMENTS FOR FULL-GATE VERIFICATION

A. Layout read-in

As a prerequisite for a full-gate verification tool, we impose the requirement that extraction must be possible from tape-out ready circuit layouts, so that circuit designers do not need to create cell copies with reduced complexity or tweaks that would otherwise impede fabrication. In this way, failure to propagate layout changes in an extraction model to the final
tape-out layout is avoided.

This is achieved by applying all port-terminal identifiers (ports can be defined as spatially separate positive and negative terminals) and operators as text labels, and defining terminal geometries and blanking areas on special layers that are not part of the fabrication process layers and therefore do not affect fabrication. Furthermore, reading in such layouts requires support for polygons without any restrictions on angles between edges, paths, and a full hierarchy of nested structures such as sub-cells that are repeated in a layout. Special layer actions must also be supported, such as the removal of objects or sections thereof below objects in the cut layer of the FLUXONICS process [15], or the creation of placeholder layers to allow the correct positioning of resistive objects in the Hypres 4.5 kA/cm² process [16].

B. Resitive layer support

Earlier versions of InductEx capable of reading full-gate layouts extracted only inductance, so that resistive sections (although processed) were not modeled. Resistors were therefore also not included in circuit netlists, although the effects of objects in a resistive layer on height offset of upper layers was modeled. This mode is still supported to allow faster inductance-only extractions when needed. Fig. 1 shows a confluence buffer from the FLUXONICS cell library, and how it is modeled for extraction when resistance is omitted. An excerpt from the solution output is shown in Fig. 2.

InductEx uses a substantially modified FastHenry [17] with superconductivity support as a numerical engine. FastHenry calculations include resistivity, so that resistive layers can be supported in InductEx. Resistive components can therefore be extracted if such objects are segmented and included in the circuit netlist, and equations for complex impedance rather than inductance are solved.

FastHenry segments are specified as resistive with the conductivity parameter “sigma”, which is the inverse of bulk resistivity $\rho$, and can be calculated from the per-square resistance and layer thickness of a resistive layer as:

$$\sigma = \frac{1}{\rho} = \frac{1}{RSd}$$

in siemens per unit length. $RS$ is the sheet resistance in $\Omega$ per square, and $d$ is the resistive layer thickness. The default unit length in InductEx is 1 $\mu$m. For the resistive layer R1 in the FLUXONICS 1 kA/cm² process, with $RS = 1$ $\Omega$ per square and $d = 80$ nm, we find from (1) that $\sigma = 12.5$ S/$\mu$m. Note that (1) does not specify the bulk resistivity of the material at room temperature, but rather the value of bulk resistivity required for FastHenry to obtain the per-square resistance for a given resistive layer and fabrication process when circuits are

<table>
<thead>
<tr>
<th>Inductor</th>
<th>Design</th>
<th>Extracted</th>
<th>AbsDiff</th>
<th>PercentDiff</th>
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<tr>
<td>L1</td>
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<td>+0.05546</td>
<td>+2.75%</td>
</tr>
<tr>
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<td>0.84519</td>
<td>+0.01519</td>
<td>+1.85%</td>
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<tr>
<td>L3</td>
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<td>2.06370</td>
<td>+0.03371</td>
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<tr>
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<tr>
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</tr>
<tr>
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</tr>
<tr>
<td>L9p2</td>
<td>0.20000</td>
<td>0.18080</td>
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</tr>
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<td>L10p2</td>
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<td>0.19488</td>
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</tr>
<tr>
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<td>+2.17660</td>
<td>+100%</td>
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</tbody>
</table>

Fig. 2. Excerpt from the solution output for the confluence buffer in Fig. 1 with the last version of InductEx before resistivity support was added (v4.14, 14 January 2013). Extracted inductance values are compared to design values.
operated at the design temperature; 4.2 K in this case.

Frequency influences skin depth in resistive conductors, but has no effect on the London penetration depth in superconducting conductors. Therefore, the frequency at which parameter extraction is performed can be set to accommodate the resistors without influencing the superconducting parts.

Adding support for the resistive layer requires different layer modelling techniques for different processes, as the isolation layers and via layouts required to create resistors vary between processes. Cross-sectional schematics for the layout of connections to resistors for three popular fabrication processes are shown in Fig. 3, and the corresponding layer setup in the InductEx layer definition file for each process is shown in Fig. 4. In order to support generic processes, InductEx allows the use of auxiliary layers, with objects copied from other layers through the “LayerADD” parameter in the layer definition file, or subtracted with the “LayerSUB” parameter [13], to model connections to resistors and lower metal layers for any resistive layer sandwich.

In the FLUXONICS 1kA/cm² process [15] (Fig. 3(a) and Fig. 4(a)), the resistive layer R1 is sandwiched between two isolation layers I1B (lower) and I2 (upper). A connection from the second metal layer M2 to R1 requires a via in I2 (which is inherently supported), while a connection between the metal layers M2 and M1 requires vias in both I2 and I1B, as well as in a lower anodization layer I1A. The layers are defined just as any other isolation and conductive layer, in ascending order of fabrication, except that a layer parameter “ViaBypass = True” is added for layer R1. This overrides the InductEx default that prohibits connections through a conductive layer if there is no object on that layer, so that a connection between M1 and M2 can be made where there is no resistive object.

In the Hypres 4.5 kA/cm² process [16], on the other hand, there is only one isolation layer (I1B) that separates metal layers M1 and M2. The resistive layer R2 is sandwiched inside I1B, so that a via in I1B can either connect M2 to R2 or to M1 (see Fig. 3(b)). In order to model this correctly in InductEx, an auxiliary isolation layer “I1BL” is defined in the layer definition file, with a process order preceding that of the resistive layer R2 and a layer thickness half that of the total isolation. The thickness of layer I1B is similarly set as half that of the total isolation. With the “LayerADD” parameter, all objects from layer I1B is copied to the auxiliary layer I1BL. The “LayerSUB” parameter is then used to delete sections of I1BL objects that overlap with R2 objects. Once again, “ViaBypass = True” is used to allow connections past the resistive layer (see Fig. 4(b)).

In the AIST STP 2.5 kA/cm² [18], [19] and ADP2 10 kA/cm² processes [20], [21], the resistive layer RES1 is sandwiched inside isolation layer GC, which also separates metal layers M1 and M2. The resistive layer R2 is sandwiched inside I1B, so that a via in I1B can either connect M2 to R2 or to M1 (see Fig. 3(b)). In order to model this correctly in InductEx, an auxiliary isolation layer “I1BL” is defined in the layer definition file, with a process order preceding that of the resistive layer R2 and a layer thickness half that of the total isolation. The thickness of layer I1B is similarly set as half that of the total isolation. With the “LayerADD” parameter, all objects from layer I1B is copied to the auxiliary layer I1BL. The “LayerSUB” parameter is then used to delete sections of I1BL objects that overlap with R2 objects. Once again, “ViaBypass = True” is used to allow connections past the resistive layer (see Fig. 4(b)).

![Fig. 3. Cross-sectional schematics of the resistive layer between two superconductive metal layers for popular fabrication processes: (a) the FLUXONICS 1 kA/cm² process, (b) the Hypres 4.5 kA/cm² process, and (c) the AIST STP and ADP2 processes. A connection between the superconductive layers is shown for each process. Layers above and below these layers are omitted for clarity.](image)

![Fig. 4. Excerpts from the layout definition files for the resistive layers and the isolation layers immediately above and below these (see Fig. 3) for popular fabrication processes: (a) the FLUXONICS 1 kA/cm² process, (b) the Hypres 4.5 kA/cm² process, and (c) the AIST ADP2 process (for AIST STP, the thickness of layer RES is 0.08 µm [19] and σ = 10.417 S/µm). Some layer parameters are omitted for brevity. Layers are defined in ascending fabrication order. The PlanarModel parameter in (c) selects the planarization method for the AIST processes.](image)
so:

InductEx uses the singular value decomposition (SVD) to do system is best solved in a least-squares sense [22], and true for any circuit other than a single inductance transmission for netlists with more than three impedances or ports. This is impedances by column for every impedance), and the vector of unknown branch currents by \( \Lambda \) (with a row for every cycle, and a column for every impedance), and the vector of unknown impedances by \( x \), then we find a system of linear equations

\[
Ax = b
\]

which is overdetermined (has more equations than unknowns) for netlists with more than three impedances or ports. This is true for any circuit other than a single inductance transmission line or a three-inductor T network. Such an overdetermined system is best solved in a least-squares sense [22], and InductEx uses the singular value decomposition (SVD) to do so:

\[
x = (A^T A)^{-1} A^T b = U A^{-1} V^T b.
\]

The particular implementation of the SVD currently used by InductEx only handles real values, which was sufficient for earlier versions when all components were purely inductive (superconducting). Resistance was ignored, so that the imaginary parts of branch current and impedance were handled as real values. However, the inclusion of resistance requires complex values for both the branch current matrix \( A \) and the impedance vector \( x \). This was solved by doubling the number of rows in \( A \) to create separate loop voltage equations for real and imaginary parts, and doubling the number columns in \( A \) and rows in \( x \) to account separately for the resistive and reactive components of branch impedance. These larger, real sets of linear equations solve correctly, at the cost of increased computer memory usage and calculation time, but remain tractable for typical circuits with fewer than 100 components.

**C. Calculation of complex impedance**

The equations solved by InductEx to calculate inductance from purely imaginary port currents [7] were also expanded to calculate impedance (resistance and inductance) from complex port currents.

The FastHenry numerical solver calculates an impedance matrix for a set of electrically isolated components, but cannot calculate impedances for a multi-port network as shown in Fig. 1(b). For this reason InductEx calculates the impedances of components in a network directly from branch currents. To do so, we modified FastHenry to write out the currents through every port when any one port is excited with a sinusoidal voltage with amplitude 1 V at an excitation frequency \( f \). InductEx also finds all closed cycles in a circuit, and keeps track of the polarity of ports and components in every cycle. Through an iterative process, the current through every branch of a circuit netlist is found from the port currents, and there are \( p \) sets of branch currents if the netlist has \( p \) ports. For every excited port, the loop voltage equation for every cycle (or mesh) is determined as the sum of the current times impedance for every branch included in a cycle (with polarities respected). The loop voltage equals \( 1 + j0 \) V or \( -1 + j0 \) V, depending on the polarity of the excited port, or 0 V if a cycle does not include the excited port. If the vector containing all loop voltages is denoted by \( b \), the matrix of branch currents by \( A \) (with a row for every cycle, and a column for every impedance), and the vector of unknown impedances by \( x \), then we find a system of linear equations

\[
Ax = b
\]

which is overdetermined (has more equations than unknowns) for netlists with more than three impedances or ports. This is true for any circuit other than a single inductance transmission line or a three-inductor T network. Such an overdetermined system is best solved in a least-squares sense [22], and InductEx uses the singular value decomposition (SVD) to do so:

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\]

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**D. Junction critical current support**

Where Josephson junction critical current \( I_C \) is a function of layout area, as it is for all popular Nb/AlO\(_x\)/Nb tunnel junction processes such as those discussed here, it is easily calculated by multiplying the junction layout area with the critical current density of the junction. In InductEx, this is supported through the addition of an “Idensity” parameter (with dimensions ampere per square unit) to the layer on which junction area is defined. For the FLUXONICS 1 kA/cm\(^2\) process, “Idensity = 1e-5” is added to the anodisation layer I1A (10 \( \mu \)A/\( \mu \)m\(^2\)), as can be seen in Fig. 4(a). For the Hypes 4-layer 4.5 kA/cm\(^2\) process, we add “Idensity = 4.5e-5” to the I1C counter-electrode definition layer, and “IDensity” for layer JJ is defined as “2.5e-5” and “1e-4” for the AIST STP 2.5 kA/cm\(^2\) and ADP2 10 kA/cm\(^2\) processes respectively.

With the layer “bias” parameter, non-zero-mean mask-to-wafer offset can be included to calculate \( I_C \) after fabrication.

**IV. FULL-GATE VERIFICATION OF FLUXONICS CONFLUENCE BUFFER**

**A. Netlist and ports**

Consider the confluence buffer discussed in Section 2A. For full-gate verification, the bias and shunt resistors need to be included in the circuit netlist, and ports must be added to the resistive branches. Inductors formed as artefacts of layout (resistive and/or inductive), and solves in 56 seconds, so that full-gate extraction here has twice the calculation cost of the inductance-only model. For RSFQ cells in general, the average solution time when resistance is modeled is 50 % to 100 % longer than for inductance-only models, while it is only around 5 % longer for circuits with low junction counts and no resistive biasing such as AQFP cells [23]. An excerpt from the solution output, which contains inductance, resistance and critical current values, is shown in Fig. 6.
It should be noted that for this extraction the segment size of resistive objects is the same as that for superconducting objects, although it can be set to different values for different layers. The inductance of resistive objects is extracted with similar accuracy to that of the superconducting objects, but at this segment size (roughly one third of the width of the resistors) the extracted resistance is high by 10% - 30%. The accuracy of extracted resistance can be made arbitrarily high through the reduction of segment size in resistive layers, at the increased cost of computation time.

C. Layout error

With full-circuit verification, some layout errors are easy to detect. As an example, consider the confluence buffer layout in Fig. 1(a). If the ground contact for junction $J_5$ between the first wiring layer M1 and the ground plane M0 is removed, inductor $L_{p5}$ in Fig. 5(a) is no longer connected to ground. Extraction yields a “no value” result for $L_{p5}$ (indicated as a double hyphen in the solution output), which indicates that $L_{p5}$ is not properly connected in the layout. Results for nearby elements are also disturbed. An excerpt from the solution output is shown in Fig. 7. The result for series components can also be seen, because with $L_{p5}$ open, $L_{J5}$ and $L_{RJ5}$ in Fig. 5(a) are in series. The total inductance and resistance of the branch is split equally between $L_{J5}$ and $L_{RJ5}$ in the solution output in Fig. 7.

Other layout errors, such as unwanted short-circuits, distort extracted impedance less obviously and are not easy to identify. We will investigate mathematical ways to identify these in future, but currently such errors are still best identified with geometry-based methods such as the layout-versus-schematic verification tool under development for the InductEx tool set [24].

V. NON-DESTRUCTIVE MODEL SIMPLIFICATION

A. Operators

InductEx supports the use of operators to allow model simplification without changes to a layout. Operators are defined in the layer definition file, and added to a layout as text labels. They act on all objects to which the text label coordinates are interior.

Currently, InductEx supports four operators. Of these, “MR,” changes all polygons on defined layers to rectangles,
which is useful for the simplification of layouts where for instance junctions are circular polygons with tens of vertices that result in unnecessarily small segments and high segment counts.

The “EC” operator creates electrical connections between nodes on two conductive layers, and removes objects on defined layers. This operator allows ground seams between multiple ground planes (or ground and sky planes) to be simplified and can result in substantial calculation speed increase.

“OD” deletes objects on defined layers, and is useful to get rid of excess structures that do not influence extraction results, while “LD” removes entire layers in for example multiple ground plane processes when lower ground planes do not influence calculation results.

Model simplification is risky, as there is always a possibility that a designer cuts away a part of a circuit that needs to be present for correct extraction. The InductEx tool set contains a utility, Inp2Dxf, with which the model files can be turned into three-dimensional representations that can be inspected visually in any viewer software that supports the DXF file format. In practice, extraction models should always be inspected in this way after a new simplification is enforced.

**B. Example with Hypres eSFQ shift register cell**

The use of operators is demonstrated for an eSFQ shift register cell [3] laid out for the 4-layer Hypres 4.5 kA/cm² process, and shown in Fig. 8. The layout includes a sky plane in the M3 metal layer for shielding.

The seams between M3 and M0 (indicated in Fig. 8(a)) require segments in layers M1 and M2, as well as vertical segments between nodes in M3, M2, M1 and M0. Since calculation time grows roughly with the third power of segment count [8], it is very efficient to trim unnecessary segments. The seams are modelled as electrical connections between nodes in M3 and M0 (rather than discrete segments) with the “EC” type operator; declared here as “GPM3M0” and

<table>
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<tr>
<th>Impedance [Ω]</th>
<th>Inductance [pH]</th>
<th>Resistance [Ω]</th>
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</thead>
<tbody>
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Fig. 9. Excerpts from the solution output for the eSFQ shift register cell in Fig. 8. (a) Solution without simplification, calculated in 1,100 seconds with a 2.9 GHz Core i7 processor, and (b) solution when ground-sky plane seams are simplified with operators, calculated in 290 seconds with the same processor.
invoked with the “@” symbol.

Without the operators to simplify the seams, the full circuit model has 38,300 segments and solves in 1,100 seconds. When the operators are used (without any changes to the layout other than adding the labels), the simulation model reduces to 27,300 segments and solves in 290 seconds. The complexity reduction and speed gain come without an accuracy penalty, as is shown in Fig. 9.

The result is that we can extract a layout with a sky plane (or even multiple ground planes) and bring calculation time to within a respectable range through the use of simplification operators, with negligible effect on accuracy if the modeling is done correctly.

C. Blanking layers

In addition to operators, the ability to cut out large swathes of layout over all layers was added to InductEx to make layout extraction easier. Any layer not used by the fabrication process can be assigned as a full or directional blanking layer (where directional blanking layers remove segments in either the x or y directions), similar to the terminal layer. Blanking layer objects therefore do not impact fabrication; only modelling. Directional blanking is used to remove segments orthogonal to the current flow direction in long lines.

D. Example of AIST-TP inductively coupled SFQ pulse transmission circuit

As an example of the use of blanking layers, consider a pulse transfer circuit [25] from the AIST STP 2.5 kA/cm² process. The circuit diagram of the pulse transfer circuit with Josephson transmission lines included is shown in Fig. 10. The size of the circuit netlist, and the separate, isolated ground planes make this extraction interesting.

Here, delimitation of the ground plane is important. The process uses a negative ground plane mask, so that InductEx fills in ground plane everywhere beneath layout structures, and up to a distance defined by the ground plane overlap parameter (set in the layer definition file) away from such layout structures. In order for InductEx to handle holes in the ground plane correctly, this ground plane fill-in surrounds ground plane holes too. In this cell layout, the moat separating the ground planes is of finite length, which requires us to enforce a border around the cell to prevent connection of the isolated ground planes during modeling. This is done with a non-fabrication blanking layer, on which an object surrounding the layout is drawn (see Fig. 11). All layers are cut away by the blanking object, which enables separated ground planes.

It can also be seen in Fig. 11 that the blanking layer is used to remove bias lines and bias line shields (which are not essential to this extraction) from the model during extraction, thereby reducing segment count and improving calculation speed; and in this case making the calculation tractable.

The circuit has 28 ports and 45 elements, resulting in 191 cycles/meshes and 5348 linear equations. The numerical calculation model has 164,000 segments and solves in 2,700 seconds while using 3.4 GB of memory.

In this layout, the mutual inductance $M_1$ between inductors $L_{CPL1}$ and $L_{CPL2}$ is an important parameter, and Fig. 13 shows
Impedance Inductance [pH] Resistance [Ω]

<table>
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<th>Name</th>
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<td>L_coil2</td>
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</table>

Mutual Inductance [pH] Coupling Factor

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Fig. 13. Excerpt from the solution output for the inductively coupled SFQ pulse transfer circuit. Mutual inductance $M_1$ is between inductors $L_{CPL1}$ and $L_{CPL2}$.

how the extraction result for $M_1$ is presented to the designer for this layout. The coupling factor is also calculated from the extracted inductance values for $L_{CPL1}$ and $L_{CPL2}$.

VI. PREPARATION OF LAYOUT FOR FULL-GATE VERIFICATION

The full-gate verification method presented here is convenient for single cell layouts such as those if Fig. 1(a) and Fig. 8(a), or for clusters with a few cells such as the layout in Fig. 11. The size of a layout is limited only by computing resources, but within the above-mentioned range, extractions take from seconds to minutes and in the largest instances around one hour on a personal computer. In this way, every cell used in a larger circuit layout can be verified individually.

Extractions are possible for much larger circuits on workstations or high performance computers with sufficient memory, but this is currently only used to find stray coupling between cells and analyze ground plane return currents.

Circuit layouts are almost always cell-based. An individual cell can be prepared for verification with InductEx by adding terminal layer objects to all peripheral inputs and outputs, and marking these as ports with labels. In rare instances, as with the split ground plane layout in Fig. 11, the cell must be demarcated by a blanking border on a non-fabrication layer. Port labels can then be added to all Josephson junctions and one terminal of every resistor, although it is not necessary to place more terminal layer objects – InductEx converts the smallest via object at a port label into a terminal. Finally, the circuit netlist must be prepared with ports connected to the correct netlist nodes to correspond to the labels on the layout. We are currently working on layout-versus-schematic extraction to automate this step.

It should be noted that coupling between any pair of inductors can be added to the netlist during extraction to identify stray coupling or bad isolation, as long as the sum of coupling and circuit elements does not exceed the number of cycles identified by InductEx for the netlist (so that (2) does not become underdetermined).

VII. CONCLUSION

Resistivity support was added to InductEx, now making it possible to verify a full cell from the tape-out ready layout (even those created with software such as LASI), and detect open connections. Junction critical current and parasitic inductance of damping resistances can also be extracted.

The inclusion of inductance branches with resistive components has another advantage: it allows the extraction of inductance and coupling from semiconductor circuits, so that hybrid circuits where semiconductor cells are in close proximity to superconducting cells can be analyzed.

Model simplification of cell layouts is possible with operators placed as text labels in layouts and objects on non-fabrication layers. The use of such simplification methods (when done correctly) reduces extraction time to seconds or minutes, with negligible effect on extraction accuracy.

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REFERENCES


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